David **Schall**

Postdoc · CPU Microarchitecture

Systems Research Group, Technical University of Munich

david.schall@tum.de | https://dhschall.github.io | dhschall | david-h-schall

Research Interest

Broad	Computer architecture, microarchitecture, prediction, memory subsystem, HW/SW codesign, sustainable computing, data center computing
Current focus	Branch prediction, cache coherence in heterogeneous architectures, reduction of misprediction cost

Education

Technical University of Munich — *Munich, Germany*

Postdoc in computer science — *01.08.2025 - present*

- Systems Research Group
- Supervisor: Dr. Pramod Bhatotia
- Research interests: CPU core microarchitecture, instruction delivery, prefetching and branch prediction

University of Edinburgh — *Edinburgh, United Kingdom*

Doctor of Science (PhD) in computer science — *01.06.2020 - 30.07.2024*

- Program: ICSA: Computer Architecture
- Supervisor: Dr. Boris Grot
- Thesis: Addressing Microarchitectural Implications of Serverless Functions [PDF]

University of Kaiserslautern — *Kaiserslautern, Germany*

Master of Science (M.Sc.) in Electronics and Information Technology — *01.04.2017 - 02.05.2019*

- Specialization: Embedded Computing Systems
- Thesis: ”Evaluation and Optimization of Memory Encryption and Integrity Protection”, In cooperation with Arm Ltd., Cambridge, UK

Heilbronn University — *Heilbronn, Germany*

Bachelor of Engineering (B.En.) in Electronics and Information technology — *01.09.2013 - 07.03.2017*

- Specialization: Information technology
- Exchange semester in South Korea, KIT Kumoh National Institute of Technology, Gumi, South Korea

Professional Experience

Arm Research, Arm Limited — *Cambridge, United Kingdom*

Master thesis and Internship — *1. Sep. 2018 - 31. Mar. 2019, 1. Feb. - 30. June 2020*

- Topic: Evaluation and Optimization of Memory Encryption and Integrity Protection.
- Modeling the encryption engine in gem5. Evaluation of system impact of encryption and integrity protection.
- Investigation and optimization of several hardware design features.
- Acquired skills: C/C++, Python and gem5

Microelectronic system design research group, University of Kaiserslautern — *Kaiserslautern, Germany*

Research Assistant — *01.08.2017 - 31.07.2018*

- Development and investigation of hardware architectures for Turbo-Code Decoders
- Writing C++ software model for Turbo-Code Decoder for performance modeling.
- Implementation and synthesis of Decoder architecture in VHDL.
- Acquired skills: C/C++, VHDL, MATLAB and Xilinx Vivado

IDS Imaging Development Systems GmbH — *Obersulm, Germany*

Bachelor Thesis — *01.09.2016 - 28.02.2017*

- Title: DisplayPort IP-Core for industry cameras
- Development of a specialized DisplayPort IP-Core for industry cameras in VHDL, based on the Xilinx Artix7 FPGA.
- Acquired skills: VHDL, MATLAB Xilinx Vivado, Xilinx FPGA’s

Bosch Engineering GmbH — *Abstatt, Germany*

Internship and Working student — *01.09.2016 - 28.02.2017*

- Hard- and Firmware development for a motor engine controller test system
- Acquired skills: C/C++, Atmel Studio, PCB design, USB firmware

Elektro Braun GmbH — *Bad Rappenau, Germany*

Apprenticeship in Electronics engineer for electrical and building services engineering — *01.09.2009 - 31.08.2012*

Teaching & Supervision

Teaching

2026	**Course Admin & Lecturer**, Introduction to Software Engineering (BSc)	*TU Munich*
2024/5	**Course Organizer**, Computer Systems Lab (BSc/MSc)	*TU Munich*
2025	**Course Organizer**, Advanced System Programming (BSc)	*TU Munich*
2020/23	**Teaching Assistant**, Introduction to Computer Systems (BSc)	*University of Edinburgh*
2023	**Teaching Assistant**, Compiler Techniques (BSc)	*University of Edinburgh*
2013	**Teaching Assistant**, Control Engineering *(original Regelungstechnik) (BSc)*	*Heilbronn University*

Supervision

since 2025	**Neel Mandal**, Reducing branch misprediction via branch recycling	*BSc Thesis*
Since 2025	**Julian Pritzi**, Verified synthesis of secure hardware	*PhD Student*
Since 2025	**Anton Ge**, Page fault forwarding via user-interrupts	*BSc + MSc Thesis*
2025	**Osman Yasa**, A top-down analysis for gem5	*Research Assistant*
2025	**Steve Bambou**, Evaluation of multiple branch prediction's potential in the context of wide-pipeline architectures	*BSc Thesis*
2025	**Phillip Assman**, Mitigating branch predictor latency with hierarchical design — an analysis	*BSc Thesis*
Since 2024	**Nicolò Carpentieri**, Coherence controllers for heterogeneous architectures	*PhD Student*
2024	**Mária Ďuračková**, Exploring hierarchical branch predictor designs	*PhD Student*
Since 2024	**Yongjie Huang**, Exploring BTB prefetching techniques	*Research Intern*
Since 2024	**L. Lakshmanan**, Microarchitectural characterization of serverless server	*Research Intern, now PhD Student*
2023	**Arun Krishna**, Building a toolchain for generating a meaningful serverless setup	*Research Intern*
2022	**Harshit Grag**, Building a serverless benchmark suite for micrarchitectural studies	*Research Intern*
2021	**Yijun Ma**, Characterizing serverless workloads	*Research Intern*

Publications

Serverless on a Server: Microarchitectural Implications of Serverless Functions — *Under submission to ISPASS 2026*

Lakshmanan Lakshmanan, Arun Krishna AMS, **David Schall**, Boris Grot — *Dec. 2025*

Guardian: Building Trusted AI Agents on Confidential Computing Hardware — *Under submission to OSDI 2026*

Teofil Bodea, Masanori Misono, Julian Pritzi, Patrick Sabanic, Thore Sommer, Harshavardhan Unnibhavi, **David Schall**, Nuno Santos, Dimitrios Stavrakakis, Pramod Bhatotia — *Nov. 2025*

vCXLGen: Automated Synthesis and Verification of CXL Bridges for Heterogeneous Architectures — *Accepted to ASPLOS 2026*

Anatole Lefort, Julian Pritzi, Nicolò Carpentieri, **David Schall**, Simon Dittrich, Soham Chakraborty, Nicolai Oswald, Pramod Bhatotia [Code] — *March. 2026*

The Last-Level Branch Predictor Revisited — *Accepted to HPCA 2026*

David Schall, Mária Ďuračková, Boris Grot [Code] — *Feb. 2026*

C^3: CXL Coherence Controllers for Heterogeneous Architectures — *Accepted to HPCA 2026*

Anatole Lefort*, **David Schall***, Nicolò Carpentieri, Julian Pritzi, Soham Chakraborty, Nicolai Oswald, Pramod Bhatotia ** equal contribution* [Code] — *Feb. 2026*

The Last-Level Branch Predictor *MICRO 2024*

David Schall, Andreas Sandberg, Boris Grot [Code] *Oct. 2024*

Warming Up a Cold Front-end with Ignite *MICRO 2023*

David Schall, Andreas Sandberg, Boris Grot [Code] *Oct. 2023*

Lukewarm Serverless Functions: Characterization and Optimization *ISCA 2022*

David Schall, Artemiy Margaritov, Dmitrii Ustiugov, Andreas Sandberg, Boris Grot [Code] *Jun. 2022*

- **IEEE MICRO TopPick's Honorable Mention**

When Does Saving Power Save the Planet? *HotCarbon, 2023*

Jackson Woodruff, **David Schall**, Michael FP O'Boyle, Christopher Woodruff *Jun. 2023*

Cryptographic Protection of Random Access Memory: How Inconspicuous can Hardening Against the most Powerful Adversaries be? *Cryptology ePrint Archive*

Roberto Avanzi, Ionut Mihalcea, **David Schall**, Héctor Montaner, Andreas Sandberg *2022*

Conference Talks

MICRO 2024, Austin, US

The Last-Level Branch Predictor [Slides] *Oct. 2024*

MICRO 2023, Toronto, Canada

Warming Up a Cold Front-end with Ignite [Slides] *Oct. 2023*

ISCA 2022, New York, US

Lukewarm Serverless Functions: Characterization and Optimization [Slides] *Jun. 2022*

Patents

Dynamic adjustment of memory for storing protection metadata *Arm Limited*

With Roberto Avanzi, Andreas Sandberg *2023*

- US Patent # US 12073104B1

Memory protection *Arm Limited*

With Roberto Avanzi, Andreas Sandberg, Ionut Mihalcea, Alexander Klimov *2023*

- US Patent # US 20240346155A1

Activities

Academic Services

Program Committee Member *2025 - PRESENT*

- ISCA '26, HPCA '26, SOCC '25, MICRO '24 Artifact Evaluation (AE), HPCA '24 AE

gem5 - Computer-system Architecture Simulator

Maintainer and Developer *2022 - PRESENT*

- Active contributor to the upstream gem5 simulator since 2022.
- Main contributions include improvements to the branch prediction model, the O3 core pipeline, and the implementation of fetch directed instruction prefetching (FDIP).
- Since 2024 maintainer mainly responsible for the O3 core and the branch predictor models.

vHive Ecosystem

Maintainer and Developer *2022 - PRESENT*

- Active developer to the vHive Ecosystem since its establishment in 2022.
- Main activities include the expansion and maintenance of the vSwarm serverless benchmark suite
- Developed vSwarm-u, a framework that integrates a serverless software stack with the gem5 simulator enabling microarchitectural research for serverless.

Ultimate Frisbee

Player and Coach *Jun. 2014 - PRESENT*

- Player in german national team (U20, U24 and Open) 2010-2016
- Assistant coach of U24 german national team 2018-2020

References

- **Prof. Dr. Boris Grot**
  Professor
  University of Edinburgh, Edinburgh, UK
  Email: boris.grot@ed.ac.uk
  Relationship: PhD Advisor

- **Prof. Dr. Pramod Bhatotia**
  Full Professor and Chair
  TU Munich, Germany
  Email: pramod.bhatotia@cit.tum.de
  Relationship: Postdoc Advisor

- **Prof. Dr. Babak Falsafi**
  Full Professor
  École d'Ingénieurs de l'Université de Lausanne (EPFL), Lausanne, Suisse
  Email: babak.falsafi@epfl.ch
  Relationship: Collaborator

- **Dr. Andreas Sandberg**
  Staff Engineer
  Arm Limited, Cambridge, UK
  Email: andreas.sandberg@arm.com
  Relationship: Internship mentor and industrial collaborator