

PhD Student · CPU Microarchitecturi

EASE Lab. University of Edinburgh

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Education

University of Edinburgh

Edinburgh, United Kingdom

Jun 2020 - present (Exp. Jun 2024)

DOCTOR OF SCIENCE (PHD) IN COMPUTER SCIENCE• Program: ICSA: Computer Architecture

- · Supervisor: Dr. Boris Grot
- · Research interests: CPU core microarchitecture, instruction delivery, prefetching and branch prediction

University of Kaiserslautern

Kaiserslautern, Germany

MASTER OF SCIENCE (M.Sc.) IN ELECTRONICS AND INFORMATION TECHNOLOGY

Apr. 2017 - Mai 2019

- Specialization: Embedded Computing Systems
- Thesis: "Evaluation and Optimization of Memory Encryption and Integrity Protection", In cooperation with Arm Ltd., Cambridge, UK

Heilbronn University

Heilbronn, Germany

BACHELOR OF ENGINEERING (B.En.) IN ELECTRONICS AND INFORMATION TECHNOLOGY

Sep. 2013 - Mar 2017

- Specialization: Information technology
- Exchange semester in South Korea, KIT Kumoh National Institute of Technology, Gumi, South Korea

Skills___

Programming Python, C/C++, Golang, VHDL

Tools gem5, ChampSim, Xilinx Vivado

Languages German, English

Experience

Arm Research, Arm Limited

Cambridge, United Kingdom

MASTER THESIS AND INTERNSHIP

Sep. 2018 - Mar. 2019, Feb. - June 2020

- Topic: Evaluation and Optimization of Memory Encryption and Integrity Protection.
- Modeling the encryption engine in gem5. Evaluation of system impact of encryption and integrity protection.
- Investigation and optimization of several hardware design features.
- Acquired skills: C/C++, Python and gem5

Microelectronic system design research group, University of Kaiserslautern

Kaiserslautern, Germany

RESEARCH ASSISTANT

Aug. 2017 - July 2018

- Development and investigation of hardware architectures for Turbo-Code Decoders
- Writing C++ software model for Turbo-Code Decoder for performance modeling.
- Implementation and synthesis of Decoder architecture in VHDL.
- Acquired skills: C/C++, VHDL, MATLAB and Xilinx Vivado

IDS Imaging Development Systems GmbH

Obsersulm, Germany Sep. 2016 - Feb. 2017

BACHELOR THESIS

• Title: DisplayPort IP-Core for industry cameras

- Development of a specialized DisplayPort IP-Core for industry cameras in VHDL, based on the Xilinx Artix7 FPGA.
- Acquired skills: VHDL, MATLAB Xilinx Vivado, Xilinx FPGA's

Bosch Engineering GmbH

Abstatt, Germany

Sep. 2016 - Feb. 2017

INTERNSHIP AND WORKING STUDENT

• Hard- and Firmware development for a motor engine controller test system

• Acquired skills: C/C++, Atmel Studio, PCB design, USB firmware

Elektro Braun GmbH Bad Rappenau, Germany

APPRENTICESHIP IN ELECTRONICS ENGINEER FOR ELECTRICAL AND BUILDING SERVICES ENGINEERING

Sep. 2009 - Aug. 2012

Publications

Warming Up a Cold Front-end with Ignite

DAVID SCHALL, ANDREAS SANDBERG, BORIS GROT

MICRO 2023

Oct. 2023

Lukewarm Serverless Functions: Characterization and Optimization

DAVID SCHALL, ARTEMIY MARGARITOV, DMITRII USTIUGOV, ANDREAS SANDBERG, BORIS GROT

ISCA 2022 Jun. 2022

• IEEE MICRO TopPick's Honorable Mention

When Does Saving Power Save the Planet?

JACKSON WOODRUFF, **DAVID SCHALL**, MICHAEL FP O'BOYLE, CHRISTOPHER WOODRUFF

HotCarbon, 2023

Jun. 2023

Cryptographic Protection of Random Access Memory: How Inconspicuous can Hardening Against the most Powerful Adversaries be?

ROBERTO AVANZI, IONUT MIHALCEA, **DAVID SCHALL**, HÉCTOR MONTANER, ANDREAS SANDBERG

Cryptology ePrint Archive

Extracurricular Activity

vSwarm - Serverless Benchmarking Suite

MAINTAINER 2022 - PRESENT

• https://github.com/vhive-serverless/vSwarm

Ultimate Frisbee

PLAYER AND COACH

Jun. 2014 - PRESENT

- Player in german national team (U20, U24 and Open) 2010-2016
- Assistant coach of U24 german national team 2018-2020